

WHAT IS CLAIMED IS:

1           1. An electromagnetic interference cancellation system comprising  
2           a control signal generation unit having a counter that counts n-bit signals to  
3           output a first output signal of n bits with a count value, and a second output signal  
4           having a level that is opposite to the first output signal, the control signal generation  
5           unit alternately outputs the first and second output signals as control signals according  
6           to a cycle of the counter;  
7           a voltage control unit that outputs a voltage having a step index level  
8           corresponding to the count value of the control signal; and  
9           an oscillator that generates a clock signal having a frequency corresponding to  
10          the voltage outputted from the voltage control unit.

1           2. The system of claim 1, wherein the counter comprises n first flip-flops that  
2           output 1 bit of the first and second output signals respectively, the flip-flops being  
3           coupled to each other in series, and

4           the first flip-flop is triggered to reverse an output at an edge where a first  
5           output signal of a previous first flip-flop becomes a first level.

1           3. The system of claim 2, wherein the control signal generation unit  
2           comprises:

3           a second flip-flop coupled to a final first flip-flop of the counter in series so as  
4           to reverse an output at an edge where a first output signal of the final first flip-flop  
5           becomes the first level; and

6           a multiplexer that alternately outputs the first and second output signals of the  
7           n first flip-flops whenever the output level of the second flip-flop is reversed.

1           4. The system of claim 3, wherein the multiplexer comprises a first  
2           transmission gate for passing the first output signal when the first and second output  
3           signals of the first flip-flop are inputted and the output of the second flip-flop is a high

4 level, and a second transmission gate for passing the second output signal when the  
5 output of the second flip-flop is a low level.

1 5. The system of claim 1, wherein the voltage control unit generates step index  
2 voltage having  $2n$  voltage levels corresponding to the count values, and the step index  
3 voltage increases and decreases according to the cycle of the counter.

1 6. The system of claim 1, wherein the oscillator receives the voltage of the  
2 voltage control unit as a high level voltage, and generates a clock signal having a  
3 frequency which is in inverse proportion to a difference between the high level  
4 voltage and a reference low level voltage.

1 7. An EMI cancellation system comprising:

2 a control signal generation unit comprising a counter having  $n$  first flip-flops  
3 that respectively output first and second output signals with opposite levels, the  $n$  first  
4 flip-flops being coupled to each other in series and each first flip-flop reversing  
5 outputs at every cycle of the first and second signals of a previous first flip-flop, a  
6 second flip-flop that outputs third and fourth output signals having opposite levels and  
7 being reversed at every cycle of the first and second output signals of a final first flip-  
8 flop of the counter, and a multiplexer for passing the first signals of the  $n$  first flip-  
9 flops as a control signal of  $n$  bits when the third output signal of the second flip-flop is  
10 a first level and passing the second output signals of the  $n$  first flip-flops as the control  
11 signal of  $n$  bits when the third output signal of the second flip-flop is a second level;

12 a voltage control unit that outputs voltages having respective step index levels  
13 corresponding to count values of  $n$ -bit control signals; and

14 an oscillator that generates a clock signal having a frequency corresponding to  
15 the step index level of the voltage of the voltage control unit.

1 8. A method for canceling electromagnetic interference by generating clock  
2 signals having various frequencies in a predetermined range, the method comprising:

3 alternately outputting an  $n$ -bit signal and a reverse signal of the  $n$ -bit signal at  
4 every cycle of the counter, the  $n$ -bit signal being counted by an  $n$ -bit counter;

5           generating an output voltage having a step index level which increases or  
6 decreases stepwise according to a count value of the control signal; and  
  
7           generating a clock signal having a frequency corresponding to the level of the  
8 output voltage.

1           9. The method of claim 8, wherein the step index level of the output voltage  
2 alternately increases and decreases according to the cycle of the counter.

1           10. The method of claim 8, wherein the clock signal is generated by an  
2 oscillator which receives the output voltage as a high level voltage such that the clock  
3 signal has a pulse width proportional to a difference between the high level voltage  
4 and a reference low level voltage.